Preliminary

Product Technical Brief
S3C6410
Rev 2.0, August. 2007

Overview

S3C6410 is a 16/32-bit RISC cost-effective, low power, high performance micro-processor solution for mobile phones, Portable Navigation Devices and other general applications.
To provide optimized H/W performance for the 2.5G & 3G communication services, S3C6410 adopts a 64/32-bit internal bus architecture and includes many powerful hardware accelerators for tasks such as motion video processing, display control and scaling. An integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG4/H.263, H.264 and decoding of VC1. This H/W Encoder/Decoder supports real-time video conferencing and TV out for NTSC and PAL mode. In addition, the S3C6410 Includes an advanced 9.3M triangles/ sec 3D graphics accelerator with OpenGL ES 1.1 / 2.0, D3DM API support

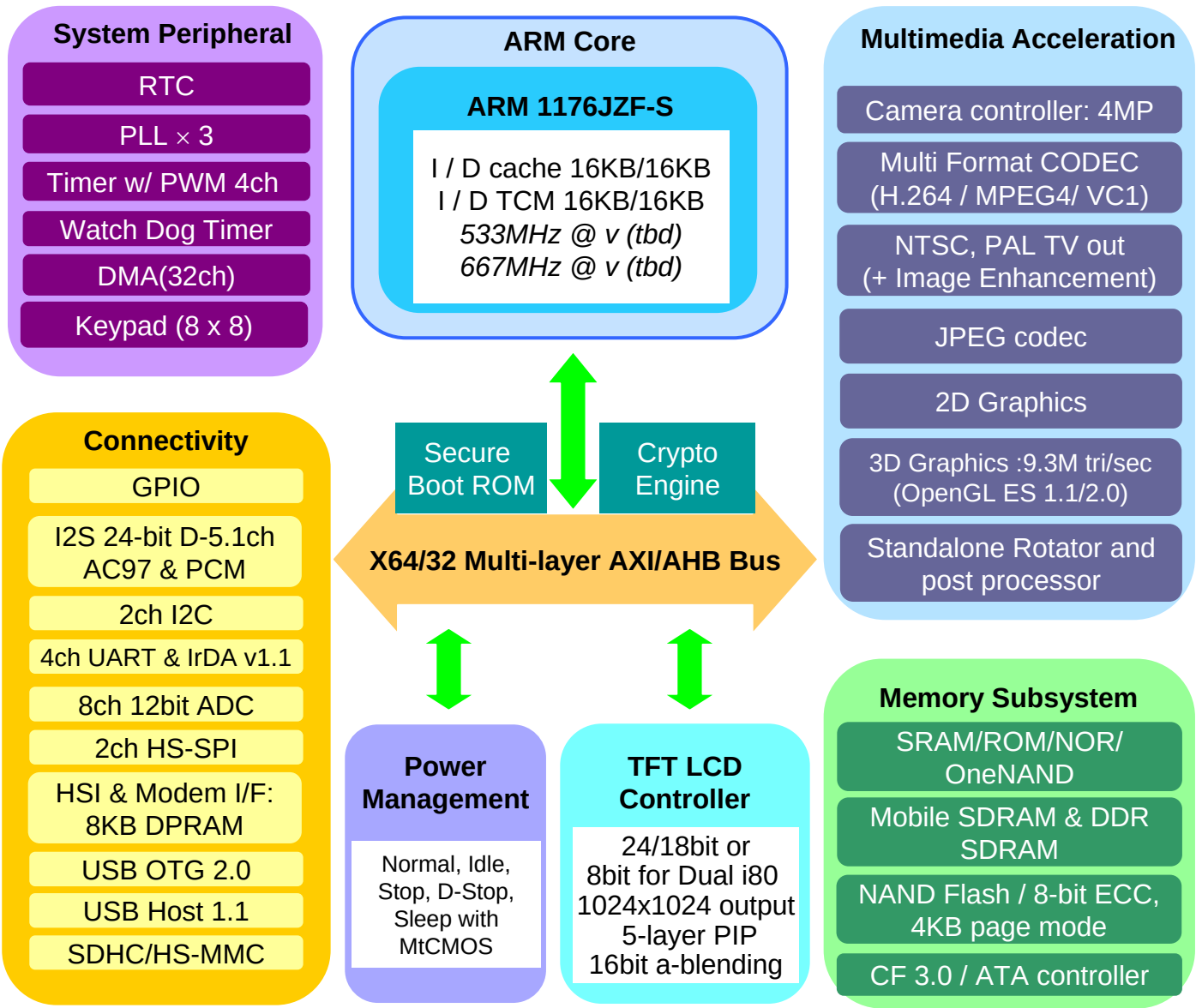
The S3C6410 has an optimized interface to external memory capable of sustaining the demanding memory bandwidths required in high-end communication services. The memory system has dual DRAM and Flash/ROM external memory ports for parallel access. DRAM port can be configured to support mobile DDR or standard SDRAM. The Flash/ROM Port supports NAND Flash, NOR-Flash, OneNAND and ROM type external memory.

To reduce the total system cost and enhance overall functionality, the S3C6410 includes many hardware peripherals such as camera interface, TFT 24-bit true color LCD controller, System Manager for power management, CF+, ATA I/F, 4-channel UART, 32-channel DMA, 4-channel Timers, General I/O Ports, I2S, I2C-BUS interface, USB 2.0 OTG controller and integrated transceiver operating at high speed(480Mbps), SD Host & High Speed Multi-Media Card Interface and PLLs for clock generation.

Furthermore, the S3C6410 is both pin and software compatible with the S3C6400 and S3C6430, thus allowing for easier migration, platformization, minimal engineering resources, and ultimately faster time to market.

The S3C6410 is manufactured using the Low Power 65nm process allowing for low power, cost sensitive applications.

POP (Package on Package) options with MCP technology are available for small form factor applications.


System Peripheral
RTC
PLL × 3
Timer w/ PWM 4ch
Watch Dog Timer
DMA(32ch)
Keypad (8 x 8)
ARM Core
ARM 1176JZF-S
I / D cache 16KB/16KB
I / D TCM 16KB/16KB
533MHz @ v (tbd)
667MHz @ v (tbd)
Multimedia Acceleration
Camera controller: 4MP
Multi Format CODEC (H.264 / MPEG4/ VC1)
NTSC, PAL TV out (+ Image Enhancement)
JPEG codec
2D Graphics
3D Graphics :9.3M tri/sec (OpenGL ES 1.1/2.0)
Standalone Rotator and post processor
Connectivity
GPIO
I2S 24-bit D-5.1ch AC97 & PCM
2ch I2C
4ch UART & IrDA v1.1
8ch 12bit ADC
2ch HS-SPI
HSI & Modem I/F: 8KB DPRAM
USB OTG 2.0
USB Host 1.1
SDHC/HS-MMC
Secure Boot ROM
Crypto Engine
X64/32 Multi-layer AXI/AHB Bus
Power Management
Normal, Idle, Stop, D-Stop, Sleep with MtCMOS
TFT LCD Controller
24/18bit or 8bit for Dual i80
1024x1024 output
5-layer PIP
16bit a-blending
Memory Subsystem
SRAM/ROM/NOR/ OneNAND
Mobile SDRAM & DDR SDRAM
NAND Flash / 8-bit ECC, 4KB page mode
CF 3.0 / ATA controller

Product Details

❒ ARM Core

- The ARM1176JZF-S processor incorporates ARM V6 architecture. It supports the ARM and Thumb™ instruction sets, and Jazelle technology for direct execution of Java bytecodes.
- A range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.
- ARM1176JZF Features
  - TrustZone™ security extensions
  - S/W Driven Power Management
  - High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced
  - Extensible Interface (AXI) level two interfaces supporting prioritized multiprocessor implementations.
  - Integer unit with integral Embedded ICE-RT logic
  - Eight-stage pipeline
  - Branch prediction with return stack
  - Low interrupt latency configuration
  - External coprocessor interface and coprocessors CP14 and CP15
  - Instruction and Data Memory Management Units (MMUs), managed using MicroTLB structures backed by a unified Main TLB
  - Instruction and data caches, including a non-blocking data cache with Hit-Under-Miss (HUM)
  - Virtually indexed and physically addressed caches
  - 64-bit interface to both caches
  - DMA
  - Vector Floating-Point (VFP) coprocessor support
  - External coprocessor support
  - Trace support
  - JTAG-based debug

❒ Memory Subsystem

- SRAM/ROM/NOR Interface
  - x8 or x16 data bus
  - Address range support: 20-bits (1MB)
  - Support byte and half-word access
- Muxed OneNAND Interface
  - x16 data bus
  - Support byte and half-word access
- SDRAM Interface
  - X16, x32 data bus
  - 1.8V interface voltage
  - Density support : up to 1Gb
  - x16 data bus with 133Mbps/pin data rate
  - Mobile SDRAM feature support :

    DS (Driver Strength Control)

    TCSR (Temperature Compensated Self-Refresh Control)

    PASR (Partial Array Self-Refresh Control)
- Mobile DDR Interface
  - x16, x32 data bus with 266Mbps/pin double data rate (DDR)
  - 1.8V interface voltage
  - Density support : up to 1Gb
- NAND Interface
  - Support industry standard NAND interface
  - x8 data bus
  - 1.8V, 2.5V, 3.3V interface voltage
  - 4KB internal buffer (stepping stone)
  - System can be booted from NAND (boot loader) when system initialization begins
  - Rest of memory area is used for storing user data
  - 1/4/8-bit hardware ECC circuit
  - 4KB page read mode support
- Secure boot and moviNAND booting by help of embedded ROM

❒ Multimedia Acceleration

■ Camera Interface

- 8-bit ITU-R601/ITU-R656 format input
- Up to 4M pixel for scaled or 16M pixel for un-scaled resolution
- YCrCb 4:2:2 to 4:2:0 down-sampling, down-scaling for MPEG and JPEG
- RGB 24-bit or 16-bit output for preview (720)
- Interlaced Input Support
- Image windowing and zoom-in function
- Test pattern generation
- Image flip supports Y-mirror, X-mirror, 180' rotation
- H/W Color Space Conversion
- LCD controller direct path supported
- Image effect supported

■ Multi Format CODEC (MFC)

- Real-time Video Encoding & decoding of MPEG4/H.263/H.264 and decoding of WMV9
- MPEG4 Up to Simple Profile : 30fps@SD(720x480)
- Supports H.263 Baseline 30fps@SD(720x480)
- H.264 Baseline Profile Level 3.0 : 30fps@SD(720x480)
- VC1 Decoding : 30fps@SD(720x480)

■JPEG Codec

- Compression/decompression up to 65536 x 65536
- Encoding format: YCbCr4:2:2 or YCbCr4:2:0
- Decoding format: YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0 or Gray

■ Rotator

- Supported image format : YCbCr 4:2:2(interleave), YCbCr 4:2:0 (non-interleave), RGB565 and RGB888(unpacked)
- Supported rotate degree : 90, 10, 270, flip vertical and flip horizontal
- Supported image size : 2048 x 2048

■2D Graphic Accelerator

- Primitive drawing engine
  - Line/Point drawing
  - Bit Block Trasfer (BitBLT)
  - Color expansion: Text drawing
- Per-pixel operation (max 2048x2048 resolution)
  - 90°/180°/270°/X-flip/Y-flip rotation
  - Window clipping
  - Rasterization
  - 256-level per-pixel alpha blending

■TV(NTSC/PAL) Encoder with Image Enhancer

- Out Video Format : NTSC-M/PAL-B,D,G,H,I Compliant
- Macrovision for anti-taping (Version 7.1.L1)
- Support source format : YCbCr420/422, RGB 16/18/24
- Built in the MIE (Mobile Image Enhancer) Engine
- Black & White Stretch
- Blue Stretch & Flesh-Tone Correction
- Dynamic Horizontal Peaking & LTI
- Black and White Noise Reduction
- Original, Full Size, Wide Size Video-Out

■ Video Post Processor

- Video input format conversion
- Video/Graphic scaling up/down or zooming in/out
- Color space conversion from YCbCr to RGB
- Color space conversion from RGB to YCbCr
- Dedicated local interface for display
- Dedicated Scaler for TV Encoder

■ 3D Graphic Accelerator

- Architecture
  - Floating-point pipeline & Object-order rendering
  - 4-Way SIMD vertex shader + pixel shader
  - Shader Model 3.0: World 1st implementation
  - 128-bit (32-bit x 4) FP x 1 Vertex Shader
    128-bit (32-bit x 4) FP x 1 Pixel Shaders
    - 8-stage pipeline
    - 512 Instruction Slots (configurable)
  - Memory BW Optimization by Hierarchical Caching
- S/W solution API
  - OpenGL ES 1.1/2.0 (Both ready internally, Khronos released 2.0 test kit in Jan'07 but confirmance test kit is not ready yet.)
  - D3D Mobile, OpenVG 1.0 (TBD)
- Rendering performance @Max frequency (133MHz)
  - Avr. triangle rate performance: 9.3M tri/sec
  - Shaded fill rate: 127M pixel/sec
  - Bilinear-filtered textured fill rate with Alpha blending: 37.8M pixel/sec
  - Vertex geometry performance: 9.28M vertices/s transform only and 7.55 vertices/s with single light

❒ Display Controller

- 24/18 bit RGB LCD Interface Support
- 8/6 bit RGB Interface Support
- Dual i80 LCD Interface Support
- 601/656 Interface Support
- 1/2/4/8bpp Palletized or 8/16/24-bpp Non-Palletized Color-TFT support
- 320X240, 640x480 or other display resolutions up to 1024x1024
- Max. 2K x 2K virtual screen size
- Support 5 Window Layer for PIP or OSD
- Realtime overlay plane multiplexing
- Programmable OSD window positioning
- 16-level alpha blending

❒ Security Subsystem

■ On-Chip secure boot ROM

- 32KB secure boot ROM for secure boot

■ H/W Crypto Accelerator

- Securely integrated AES, DES/3DES, SHA-1/MD5, RNG

■ ARM TrustZone™

- Enabling enhanced secure platform for separate (secure/non-secure) execution environment for security sensitive application

❒ Connectivity

■ I2S Bus Interface

- 3-ch I2S-bus for the audio-codec interface with DMA-based operation
- Serial, 8/16/20/24-bit per channel data transfers
- Supports I2S, MSB-justified and LSB-justified data format
- Various bit clock frequency and codec clock frequency support
  - 16, 24, 32, 48 fs of bit clock frequency
  - 256, 384, 512, 768 fs of codec clock frequency
  - Multi channel Audio I/F support up to 5.1

■PCM Audio I/F

- 16-bit mono audio I/F
- Master mode only

■AC97 Audio I/F

- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In.
- 16-bit stereo(2-channel) audio.
- Variable sampling rate AC97 Codec interface (48KHz and below)

■ Modem I/F

- Asynchronous direct and indirect 16-bit SRAM-style interface (support i80 style)
- On-chip 8KB dual-ported SRAM buffer for direct interface
- On-chip Write/Read FIFO (each 288-word) to support indirect burst transfer

■ HSI

- MIPI Standard Draft Compliant
- High speed synchronous serial interface

■ CF+/ATA controller

- CF+ and CompactFlash Spec 3.0 compatible including ATA6 (except MDMA operation)

■ I2C Bus Interface

- 2-ch Multi-Master I2C-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode
- Up to 400 Kbit/s in the fast mode

■UART

- 4-channel High-Speed UART (4Mbps) with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Supports external clock for the UART operation (UCLK)
- Programmable baud rate
- Loop back mode for testing
- Non-integer clock divides in Baud clock generation (BRM)

■ IrDA

- IrDA v1.1 support (1.152Mpbs and 4Mpbs)
- SIR(111.5kbps) mode is supported by the UART IrDA 1.0 block
- Internal 64-byte Tx/Rx FIFO

■ USB OTG 2.0

- Complies with the USB OTG 2.0
- Supports high speed up to 480Mbps
- On-chip USB transceiver

■ USB Host 1.1

- Complies with the USB 1.1
- Supports full speed up to 12Mbps
- On-chip USB transceiver

■ **HS-MMC/SDIO**
- Multimedia Card Protocol version 4.2 compatible (HS-MMC)
- SD/SDIO Memory Card Protocol version SDA spec version 2.0 compatible
- SDHC (SD High Capacity) card support
- DMA based or Interrupt based operation
- 512 Bytes (HS-MMC) and 64 Bytes (MMC) FIFO for Tx/Rx: 128 word FIFO for Tx/Rx
- CE-ATA support
- 3-ch SD/SDIO/MMC or
- 1-ch HS-MMC/SDHC & 1x SD/SDIO/MMC

■ **SPI Interface**
- 2-ch Serial Peripheral Interface Protocol with full-duplex: up to 50Mbps
- DMA-based or interrupt-based operation

■ **Keypad**
- 8x8 Key Matrix support
- Provides internal de-bounce filter

■ **A/D Converter and Touch Screen Interface**
- 8-ch multiplexed ADC
- Max. 500K samples/sec and 12bit resolution

■ **Configurable GPIO (TBD)**

❒ System Peripheral

■ Real Time Clock

- Full clock features: sec, min, hour, date, day, week, month, year
- 32.768 KHz operation
- Alarm interrupt
- Time-tick interrupt

■ PLL

- Three on-chip PLLs, APLL/ MPLL / EPLL
- APLL dedicates to ARM core
- MPLL generates the system reference clock
- EPLL generates clocks for the audio interface

■ Timer with Pulse Width Modulation

- 4-ch 32-bit Timer with PWM
- 1-ch 32-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Support external clock source

■ 16-bit Watch Dog Timer

■ DMA

- 4 General DMA embedded. 8 channel supported per each DMA so then totally 32 channel is supported
- Memory to memory, IO to memory, memory to IO, and IO to IO support
- Burst transfer mode to enhance the transfer rate

■ Vectored Interrupt Controller

- multiple interrupt request inputs, one for each interrupt source, and one interrupt request output for the processor interrupt request input
- software can mask out particular interrupt requests
- prioritization of interrupt sources for interrupt nesting.

■Power Management

- Clock-off control for individual components
- Intelligent Power Gating of Multiple Power Domains to switch of unused blocks.
- Various power-down modes are available such as Slow, Idle, Stop, Deep-Stop and Sleep mode
- Wake-up by one of external interrupts or by the RTC alarm interrupt
- Step-by-Step “Noise Aware” Wake-up Design
- MtCMOS Technology
- Memory/Logic Retention

❒ Electrical Characteristics

■ Operating Conditions

- Supply voltage for core
  - 533MHz @1.2V (tbd)
  - 667MHz (target) @ tbd
- Supply voltage for logic
  - 533MHz @1.2V (tbd)
  - 667MHz (target) @ tbd
- Supply voltage for Alive/PLL: 1.2V (tbd)
- External memory port 1: 1.8V ~ 3.3V (tbd)
- External memory port 2: 1.8V ~ 2.5V (tbd)
- External IO interface: 1.8V ~ 3.3V (tbd)